Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-4. (Canceled)

5. (Currently amended) A method of performing calculations and data transfers, comprising:

receiving input data into a second register at a first time,

transferring the input data from the second register to a first register at a second time,

performing arithmetic operations in a processor substantially continuously, the arithmetic operations including functional operations applied to the input data in the first register to produce therefrom output data, and dummy operations,

transferring the output data ~~between~~ from the processor ~~and a~~ to the first register, ~~the data including select data associated with the functional operations and dummy data associated with the dummy operations,~~

~~selectively~~ transferring the ~~select~~ output data ~~between~~ from the first register ~~and a~~ to the second register at a third time, and

transferring the ~~select~~ output data ~~between~~ from the second register ~~and~~ to an other component at a fourth time,

wherein the dummy operations are performed during gaps in the functional operations so as to mask the power consumption associated with the functional operations, and the segregation of the second and third times from the first and fourth times serves to mask data transfer operations.

6. (Currently amended) The method of claim 5, wherein

~~transferring the select data between the second register and the other component is performed at a time that is~~ the first and fourth times are uncorrelated with performing the functional operations~~, so as to prevent a determination of a correlation of power consumed while performing the functional operations and power consumed while transferring the select data between the second register and the other component~~.

7. (Previously presented) The method of claim 5, wherein

the functional operations correspond to a cryptographic algorithm.

8. (Currently amended) The method of claim 5, wherein

performing the arithmetic operations, transferring the input data to the first register, and transferring the ~~select~~ output data to the second register are arranged to substantially mask power consumption related to performing the functional operations.

9. (Currently amended) The method of claim 5, wherein

performing the arithmetic operations~~,~~ and transferring the input and output data~~, and transferring the select data~~ are arranged to consume substantially uniform power consumption.

10. (Currently amended) An integrated circuit comprising:

a processor,

a first data register that is coupled to the processor,

a second data register that is coupled to the first data register and ~~is configured to transfer data between the first data register and the second data register and between the second data register and~~ to an other component, and

a controller,

wherein

the processor is configured to:

perform a given set of functional operations to execute an intended algorithm ~~during a first time sequence~~, based on input data in the first data register, and

transfer output data ~~between~~ from the processor ~~and~~ to the first data register while performing the given set of functional operations; ~~and~~

the controller is configured to:

transfer the input data from the second data register to the first data register and the output data from the first data register to the second data register according to a first time sequence,

transfer the input data from the other component to the second register and the output data from the second register to the other component according to a second time sequence; and

the second time sequence ~~control the transfer of data at the second register in a second time sequence that~~ is substantially uncorrelated with the first time sequence~~, so that a correlation of first currents associated with performing the given set of functional operations and second currents associated with performing the data input and data output transfers related to the given set of functional operations cannot be determined~~.

11. (Currently amended) The integrated circuit of claim 10, wherein

the processor is further configured to execute dummy operations that do not affect the ~~select~~ output data during gaps in ~~the first time sequence~~performing the functional operations.

12. (Previously presented) The integrated circuit of claim 11, wherein

the controller is further configured to control the processor to perform the dummy operations during the gaps in the functional operations.

13. (Currently amended) The integrated circuit of claim 12, wherein

the controller is configured to control the processor and to transfer the input and output data so as to substantially mask power consumption variations related to the functional operations.

14. (Currently amended) The integrated circuit of claim 12, wherein

the controller is further configured to transfer dummy data that does not affect the ~~select~~ output data between the first register and the second register.

15. (Currently amended) The integrated circuit of claim 14, wherein

the controller is configured to control the processor and to transfer the input, output, and dummy data so as to substantially mask power consumption variations related to the functional operations.

16. (Previously presented) The integrated circuit of claim 10, wherein

the intended algorithm is a cryptographic algorithm.

17. (Currently amended) An apparatus comprising:

a processor that is configured to perform a sequence of functional operations related to a set of input data to produce therefrom a set of output data,

a first register that is configured to provide input data and output data storage capabilities for the processor to perform the sequence of functional operations,

a second register that is configured to facilitate transfer of the sets of input data and output data between the ~~processor~~ first register and an ~~other~~ external component, and

a controller that is configured to control ~~the~~ transfers of the sets of input and output data ~~between~~ among the first register, the second register, and the external component,

wherein

the controller is configured to ~~provide the transfer of the set of data between the second register and the external component by controlling a~~ control transfer of the set of input data ~~between~~ from the second register ~~and~~ to the first register, so that the processor can perform the sequence of functional operations related to the set of input data at the first register, and

the controller is further configured to control ~~the~~ transfer of the set of output data ~~between the second register and~~ from the first register to the second register so that the transfer of the sets of input and output data between the second register and the other component is substantially uncorrelated to the sequence of functional operations performed by the processor.

18. (Previously presented) The apparatus of claim 17, wherein

the sequence of functional operations performed by the processor corresponds to a cryptographic algorithm.

19. (Currently amended) The apparatus of claim 17, wherein

the processor is further configured to perform other operations that are unrelated to the ~~transfer of the set of data between the first register and the second register~~ functional operations, so as to mask power consumptions related to the sequence of functional operations performed by the processor.

20. (Previously presented) The apparatus of claim 17, wherein

the processor is further configured to perform other data transfer operations that are unrelated to the transfer of the set of data between the first register and the second register, so as to mask power consumptions related to the transfer of the set of data between the first register and the second register.